International Journal of Electrical and Electronics Research ISSN 2348-6988 (online)
Vol. 3, Issue 3, pp: (177-180), Month: July - September 2015, Available at: www.researchpublish.com

VLSI Implementation of MIMO

[1]Ms. Komal pokale, [2]Prof. Shrikant Ahirwar, [3]Prof. Gudla Ramalakshmi

[1]M.Tech Scholar , [2]HOD, [3]Associat Professor

[1,2,3] Deptt. Electrical Engineering Bhabha College of Engineering Bhopal- 462033(M.P.)

Abstract: **The Multiple Input Multiple Output (MIMO)-Orthogonal Frequency Division Multiplexing (OFDM) is considered a key technology in modern wireless-access communication systems. The IEEE 802.16e standard, also denoted as mobile WiMAX, utilizes the MIMO-OFDM technology and it was one of the first initiatives towards the roadmap of fourth generation systems. This paper presents the PHY-layer design, implementation and validation of a high-performance real-time 2x2 MIMO mobile WiMAX transmitter that accounts for low-level deployment issues and signal impairments. The focus is mainly laid on the impact of the selected high bandwidth, which scales the implementation complexity of the baseband signal processing algorithms. The latter also requires an advanced pipelined memory architecture to timely address the datapath operations that involve high memory utilization.**

Keyword: **MIMO, OFDM, FFT.**

I. INTRODUCTION

1.1 Multiple-input multiple-output (MIMO):

The growing demand of data, multimedia and communication has requested the need for generating many disparate devices into a high speed and efficiency bandwidth network capacity, with seamlessly supporting and integrating each sector's unique requirements. The multiple-input multiple-output (MIMO) schemes have been widely studied and received great attention by both academy and industry in wireless communications application. The application of multiple antennas at both transmitter and receiver provides enhanced performance over diversity system. This technique can significantly increase the data rates of wireless system without increasing system power or bandwidth.

1.2 Orthogonal Frequency Division Multiplexing (OFDM):

OFDM is modulation method known for its capability to mitigate multipath. It can provide a flat with the sub-carrier, and achieve high efficiency and ability to deal with frequency selective fading and narrowband interference. Also the flexibility using MIMO with OFDM can support the non-flat fading channels.

Multiple input, multiple output-orthogonal frequency division multiplexing (MIMOOFDM) is the dominant air interface for 4G and 5G broadband wireless communications. It combines multiple input, multiple output (MIMO) technology, which multiplies capacity by transmitting different signals over multiple antennas, and orthogonal frequency division multiplexing (OFDM), which divides a radio channel into a large number of closely spaced sub channels to provide more reliable communications at high speeds. Research conducted during the mid-1990s showed that while MIMO can be used with other popular air interfaces such as time division multiple access (TDMA) and code division multiple access (CDMA), the combination of MIMO and OFDM is most practical at higher data rates.

MIMO-OFDM is the foundation for most advanced wireless local area network (Wireless LAN) and mobile broadband network standards because it achieves the greatest spectral efficiency and, therefore, delivers the highest capacity and data throughput. Greg Rayleigh invented MIMO in 1996 when he showed that different data streams could be transmitted at the same time on the same frequency by taking advantage of the fact that signals transmitted through space bounce off objects (such as the ground) and take multiple paths to the receiver. That is, by using multiple antennas and precoding the

data, different data streams could be sent over different paths. Raleigh suggested and later proved that the processing required by MIMO at higher speeds would be most manageable using OFDM modulation, because OFDM converts a high-speed data channel into a number of parallel, lower-speed channels.

1.3 FFT:

The FFT processor is one of the kernel modules having high computational complexity in the physical layer of the MIMO-OFDM system, which is used to process multicarrier modulation. Since the MIMO-OFDM system needs more independent channel operators and processors, the system complexity and hardware cost dramatically increase.

The main goal of this project is to design high-speed, low-complexity 128/64-point FFT processor with a four-parallel data-path and a multipath delay feed-back (MDF) structure to deal with the issues of the high-throughput and hardware complexity for MIMO-OFDM applications. It can provide a higher throughput rate and low hardware complexity.

II. METHODOLOGY

The multiple-input multiple-output (MIMO) schemes have been widely studied and received great attention by both academy and industry in wireless communications application. The application of multiple antennas at both transmitter and receiver provides enhanced performance over diversity system. This technique can significantly increase the data rates of wireless system without increasing system power or bandwidth. The MIMO scheme has been adopted by the IEEE 802.11n Wireless LAN and IEEE 802.16e WiMAX standards [2]. Orthogonal Frequency Division Multiplexing (OFDM) is modulation method known for its capability to mitigate multi path.It can provide a flat with the sub-carrier, and achieve high efficiency and ability to deal with frequency selective fading and narrowband interference. Also the flexibility using MIMO with OFDM can support the non-flat fading channels [3].

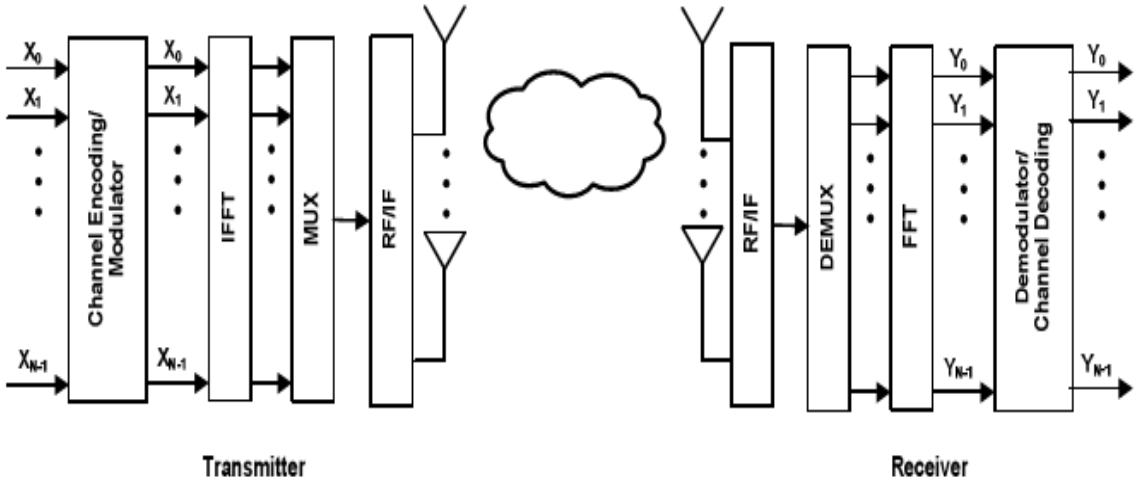

Figure 2. 1 General transreceiver of MIMO-OFDM system [3]

The IFFT and the FFT are used for, respectively, modulating and demodulating the data constellations on the orthogonal subcarriers[1] .One of the key components in OFDM system is the Fast Fourier Transform (FFT). There are more and more communication systems require higher points FFT and higher symbol rates. FFT also finds applications in linear filtering, digital spectral analysis and correlation analysis, Ultra Wide Band (UWB) applications etc. [4]. The complete MIMO-OFDM processing is implemented in a system with two transmit and two receive FFT processor i.e.64 FFT processor and 128 FFT processor. FFT can be design by following ways - 1)FFT Architecture 2)FFT Algorithm.

2.1 FFT Architecture:

There are different architectures of FFT processor to perform 64 point and 128 point FFT analysis.

2.1.1 Parallel FFT Architecture:

Parallel FFT architecture based on Cooley-Tukey algorithm provide high throughput. Multiple pipeline FFT processors using time-multiplexing are utilized to perform FFT computation tasks in parallel. This design realizes high performance using task-level parallelism and avoids complex routing. Furthermore, to reduce the memory power consumption, a

periodic memory activation (PMA) scheme is developed.By adding more processing elements to the processor in each sequential pipeline stage, performance can be improved even further. The butterflies can then be computed in parallel in any stage. The total execution time for the parallel iterative processor is log 2 *N* cycles. [6]

2.1.2 Pipeline Architecture:

Pipeline FFTs are a class of parallel algorithms that contain an amount of parallelism equal to log *R N* where *N* is the number of points for an FFT and *R* is the radix. A Pipeline implementation of the FFT was first proposed which consisted of a series of computational blocks each composed of delay lines, coefficient storage, commutators, multipliers, and adders.

Pipeline FFTs can be generally run at high-speeds and the amount of pipelining increased or decreased to meet timing. Different pipeline approaches and put into functional block with unified technology. To improve the performance of the sequential processor, parallelism can be introduced by using a separate arithmetic unit for each stage of the FFT. This increases the throughout by factor of log 2 *N* when the different units are pipelined. This architecture is also known as cascaded FFT architecture and will be used in proposed design.[10]

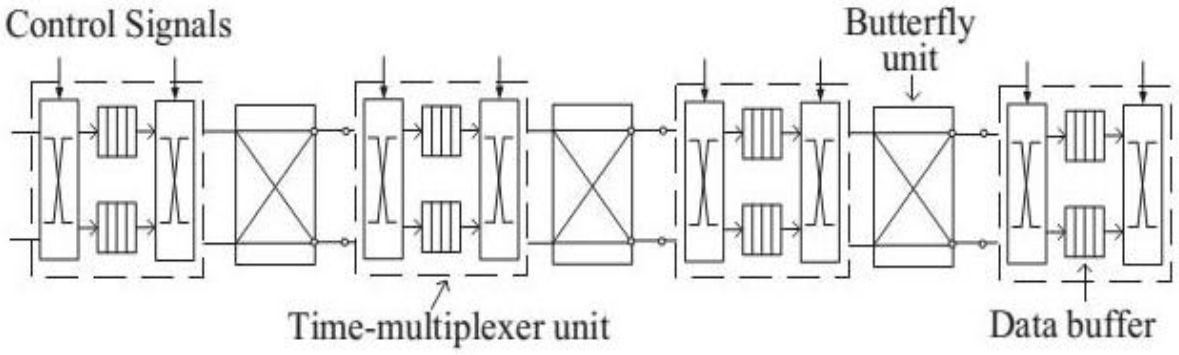

Figure 2.1.2 Pipeline FFT Architecture [5]

There are 2 types of pipeline FFT Architecture:-

2.1.2.1 Single path delay feedback [SDF]:

Single- path Delay Feedback uses the registers more efficiently by storing one output of each butterfly in feedback shift registers. A single data stream goes through the multiplier at every stage. It has same number of butterfly units and multipliers as in MDC approach, but with reduced memory requirement:N-1registers.Its data throughput is (1/x) times that of the corresponding MDC architecture. Advantage of single path delay feedback is its required less area.

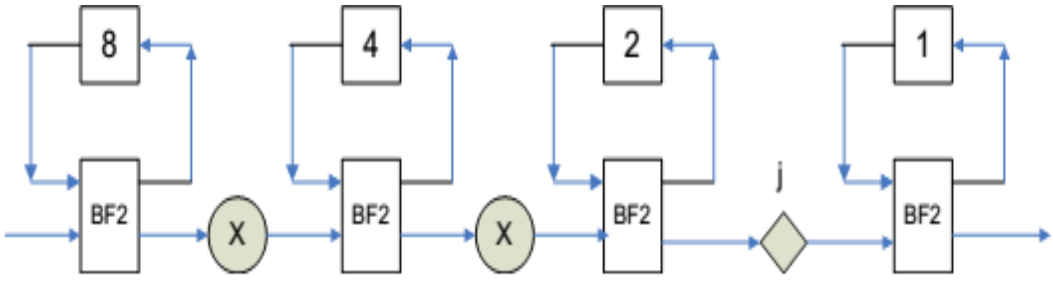

Figure 2.1.2.1:- 4 Single path delay feedback [11]

2.1.2.2 Multipath delay commutator [MDC]:-

Multi-path Delay Commutator is the most classical approach for pipeline implementation of radix-2 FFT algorithm. As shown in Fig. the input sequence has been broken into two parallel data stream flowing forward, with correct distance between the data elements entering the butterfly scheduled by proper delays. Both butterflies and multipliers are in 50% utilization. In certain applications like Multiple input Multiple output (MIMO) systems, The first commutator at the input data stream can be replaced with 2 such commutators to keep the pipeline components 100% utilized. The output data rate for this structure is twice the clock frequency and that is what makes it appealing for high-speed applications.

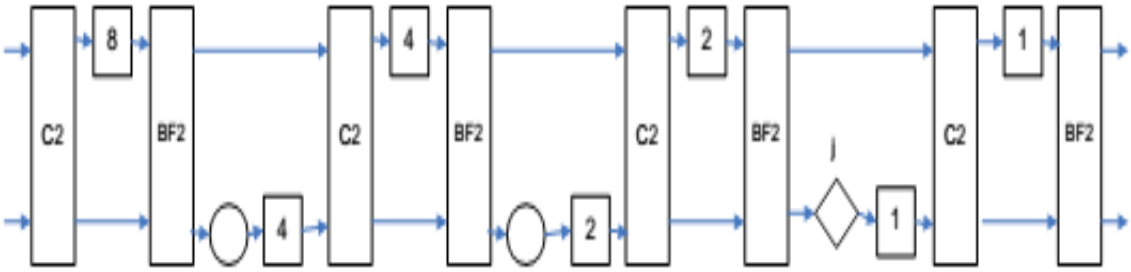

Figure 2.1.2.2:- 5 Multipath delay commutator [MDC][11]

FFT processor using different architectures that allows any size points to transform, fixed point arithmetic, pipeline structure and parameterized data format[11].

III. CONCLUSION

In this project, we designed an OFDM receiver with different FFT algorithms and they are implemented using VLSI design process. It was found during the algorithm design that many blocks need complex multipliers and adders and therefore special attention needs to be given to optimize these circuits and maximize reusability. In particular, the models have been applied to analyze the performance of mixed-radix FFT architectures used in OFDM. Actual hardware resource requirements were also presented and simulation results were given for the synthesized design. The 64-point Mixed-Radix 4-2 FFT based OFDM architecture was found to have a good balance between its performance and its hardware requirements and is therefore suitable for use in OFDM systems.

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